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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,099	01/14/2002	Hiroshi Moriya	500.41080X00	6738

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,099	MORIYA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *18 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *12-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Response to Amendment

This Office Action is in response to Applicants' amendment filed on March 18, 2003.

Therefore claims 12 – 16 as originally filed and claims 17-24 presently newly added are currently pending in the application. Claims 1-11 have been cancelled by the amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17, 21 and 24 are rejected under 35 U.S.C. 102(b) as being obvious over Japanese patent Publication No. 53010282 (herein after Matsushita).

With respect to claims 17, 21 and 24, Matsushita describes a semiconductor device including a semiconductor substrate Abstract line 1 all MOS transistors have a semiconductor substrate), gate insulators formed on said substrate and gate electrodes formed on said insulators (Basic abstract), wherein said gate insulators are composed of a material as a main component selected from titanium oxide, zirconium oxide and hafnium oxide (Basic abstract lines 3-5)

and in which compression strain is produced (Basic abstract line 9-10) , said semiconductor device equipped with Mos transistors. (Abstract line 1).

With respect to claim 21 wherein the insulator comprises a film mainly composed of silicon oxide and an overlying film mainly composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide (Matsushita page 438 line 7 from the bottom left hand side coloum. (for response to Applicants' arguments see response to arguments section below).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 18-20, 22-23 and 12-15 are rejected under 35 U.S.C. 103(a) and further in view of Van Dover (U.S. Patent No. 6093944 herein after Van Dover).

With respect to claims 18, 20 Matsushita describes a semiconductor device including a semiconductor substrate, gate insulators formed on the substrate and gate electrodes formed on the gate insulators as stated above.

Matsushita does not specifically describe or teach the gate insulator layer is mainly composed of titanium oxide having a retile crystal structure.

However, Van Dover a patent from the same field of endeavor, describes in fig.2 and col. 1 lines 53-56 describes Titanium oxide as gate oxides and col. 6 lines 27-29 for retile) to form (TiO2) dielectric films having sufficiently low leakage currents for reliable use in DRAM devices.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Andover's titanium oxide in Matsushita's device to form (TiO2) dielectric films having sufficiently low leakage currents for reliable use in DRAM devices.

In which compression strain is produced, and said semiconductor device equipped with Mos transistors (see above under claim 1 above, (Basic abstract line 9-10 Abstract line 1).

Claim 20 further specifies that tensile strain is produced in the gate insulator and tensile strain is produced in the gate electrode (Matsushits describes all types of strain including both the compression and tensile strains being produced in both the gate insulators and the gate electrode)

With respect to claim 19, it repeats all the steps of claim 18 and further adds wherein the thermal expansion coefficient of the main composing material of the gate electrodes is greater than the liner coefficient of the titanium oxide.

Matsushita and VanDover describes all the steps of that are repeated from claim 2 as shown above.

Further VanDover describes a ploy silicon gate in col. 4 lines 40-45 similar to that described in Applicants' specification page 14 lines 3-8 in the same context and for the same purpose and therefore what is true for applicants' (their polysilicon gate wherein the thermal expansion coefficient of the main composing material of the gate electrodes is greater than the liner coefficient of the titanium oxide) is also true for VanDover's polysilicon gate.

With respect to claim 22, it repeats all the steps of claim 18 and further adds that a second MOS transistor has a gate insulator containing silicon oxide in a high proportion. (Matsushita page 438, Van Dover fig.1)

With respect to claim 23, it repeats all the steps of claim 18 and further adds that the first MOS transistor is used for calculations or memories and the second MOS is used for I/O. (Van Dover – Dram or memory device having a memory circuit (calculations or memories) and a peripheral circuit (Imput/Output i.e. I/O).

With respect to claim 24, it repeats all the steps of claim 17 and further adds that the gate insulator has a multiplayer structure (Van Dover fig. 1).

With respect to claim 12, it repeats all the steps of claim 18 and further adds that the main crystal structure of the titanium oxide is anatase (Van Dover col.6 line 29) and the state of strain of the channel region of said semiconductor substrate is tensile strain. (Matsushita Abstract 4th line from last).

With respect to claim 13, wherein a silicon oxide film or a titanium silicate film is deposited between the semiconductor substrate and said titanium oxide gate insulator (Van Dover col. 4 lines 45-50).

With respect to claim 14, wherein the gate electrodes have a phosphorus or boron-added polycrystalline silicon film, (Van Dover claim 7) and a silicon oxide film or a titanium silicate film is inter posed between the gate electrodes and the titanium oxide gate insulators. (Van Dover col. 4 lines 45-50).

With respect to claim 15, wherein the gate electrodes include a tungsten film, a molybdenum film, a tungsten nitride film, a tungsten boride film, a tungsten silicide film or a laminate thereof (Van Dover Van Dover col. 4 lines 50-55).

B. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita as applied to claims 1,5,9 and 11 above and further in view of Van Dover (U.S. Patent No. 6093944 herein after Van Dover). And Lau (U.S. Patent No. 6,249 0898, herein after Lau).

With respect to claim 16, wherein the gate electrodes include a ruthenium oxide film, which is in contact with the titanium oxide gate insulator.

Matsushita and VanDoren do not specifically describe a gate electrode to include ruthenium oxide.

However, Lau, a patent from the same field of endeavor describes in col. 5 line 8

Describes a gate electrode of ruthenium oxide to repair the pinholes in the oxide insulator layers which lead current leakage in the device.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Lau's gate electrode of ruthenium oxide in Matsushita and VanDover's device to repair the pinholes in the oxide insulator layers which lead current leakage in the device.

Response to Arguments

Applicant's arguments filed 3/18/2003 have been fully considered but they are not persuasive. for the following reasons.:

Applicants' first contention that Matsushita fails to teach or suggest any treatment (i.e. conditions are set) to provide compression strain in the material of the gate insulators is not persuasive because, the claims in consideration are device claims that do not recite any of the treatment (conditions set) and what is not recited in the claims need not be given patentable weight.

Further it is noted that all the structural limitations recited by the claims including the compression strain (inherently disclosed) are described by the Applied Matsushita reference.

Applicants' next argument with respect to claims 18 and 20 that neither Matsushita or Van Dover teach or suggest compression strain is reduced is also not persuasive because as shown above Matsushita describes compressed/ compression strain and further as previously stated, Matsushita in English Abstract (Basic Abstract Section) 4 th line from bottom states " less strain".

Applicants' next contention that Claim 22 is allowable because the applied reference does not teach two different transistors with two different gate insulators is also not persuasive because Van Dover in col. 4 lines 45-47 describes silicon dioxide gate insulator and gate insulating film of TiO_2 i.e gate insulators of two different material.

Applicants' next contention that claims 12 to 16 be allowed because allegedly the prior art does not teach the crystal structure of titanium oxide is

anatase and the state of strain of the channel region of said semiconductor substrate is tensile strength is not persuasive for reasons set out under claim 17,21,24 above.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

May 30, 2003.